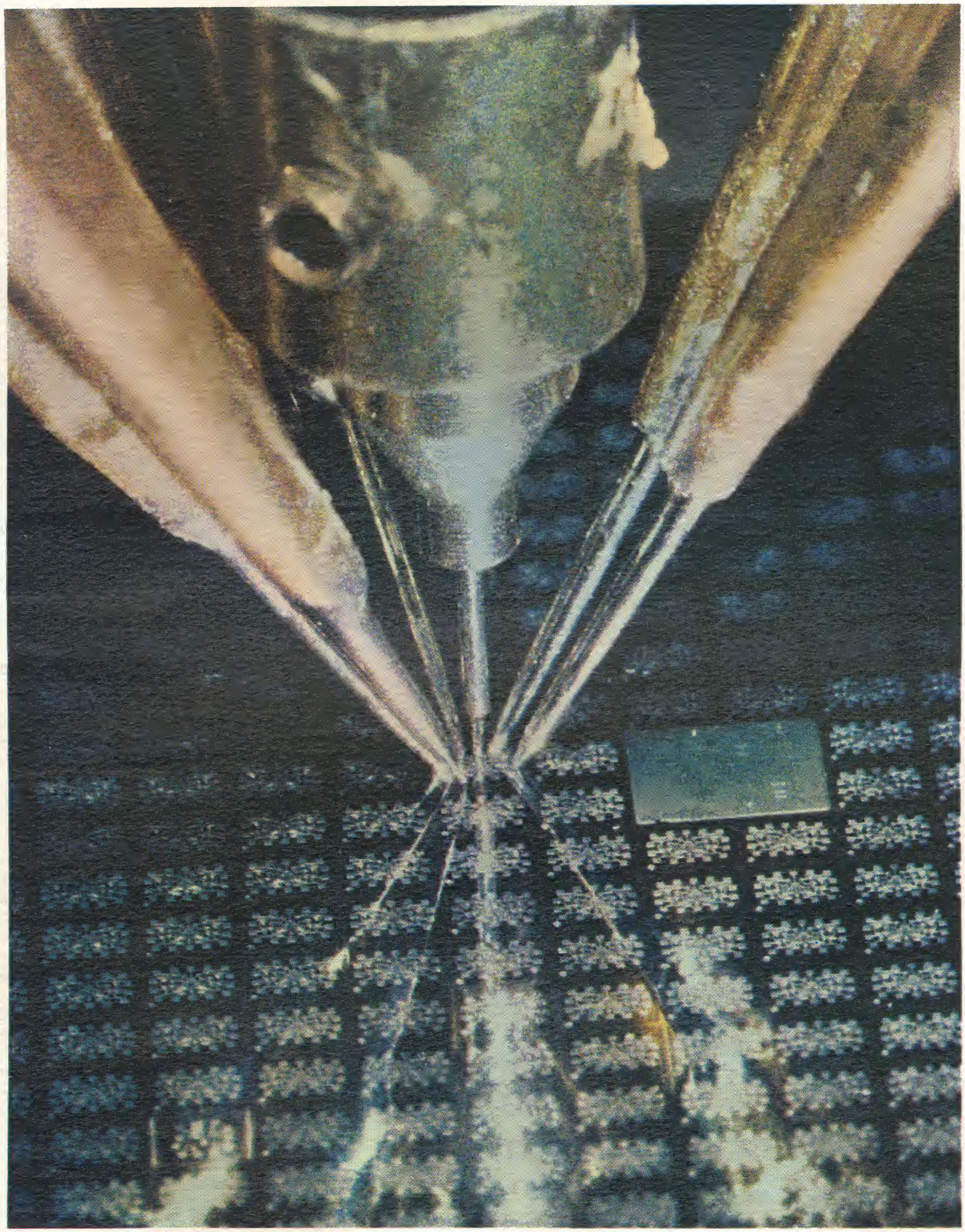


3C PULSE

Special Microcircuit Issue

MICROCIRCUIT LOGIC MODULE CAPABILITY

Since introduction ten years ago of the first 3C PAC®, Computer Control Company, Inc., has designed, manufactured and delivered over one million discrete digital logic modules. These have met both general and special purpose needs of the military, government and industry for modular building block logic circuits. From early vacuum tube circuits, to the first transistorized circuits and the innovation of NAND operation, to uniquely designed and packaged circuits currently aboard the JPL/-NASA Mariner vehicle enroute to Mars, 3C has made a total commitment to the design and manufacture of an extensive range of electrically, mechanically and logically complete circuit module lines. The success of these applied circuit design and packaging capabilities is due to the user orientation of all development efforts. This sensitive awareness to user needs for flexibility and reliability has in large measure grown out of 3C experience with its own general and special purpose systems business.

The company's first module line was the 1 mc vacuum tube V-PAC developed in 1955. The following year 3C introduced 100 kc M-PACS, the first commercially available fully transistorized digital circuit module. In 1957 1 mc T-PAC was announced, featuring synchronous dynamic logic and packaging economies. To this day, T-PAC sales still represent a significant contribution to the company and the industry. Three years later H-PAC became the first commercially available clocked 20 mc digital module line. This same line included unique serial memory glass delay line modules which have become one of the most popular features of this active module line. Shortly after the H-PAC introduction, 3C released S-PAC, a 1 mc, 5 mc, and 200 kc family of modules with over 150 standard models, extensive hardware options, design aids and specials. If there is an industry standard today, S-PAC which has achieved the largest single share of the module market, best represents that standard.

Late in 1960, parallel to these commercially-oriented developments, 3C embarked on a development program to produce low power, high density digital circuits and, ultimately, pellet components for JPL/NASA scientific Mariner Venus, Mariner Mars and Ranger space probes. Unique packaging techniques developed for these programs led to the design of forerunners to 3C's new μ-PAC integrated circuit module line.

Almost two years ago during early developments in microcircuit technology — the fabrication of smaller, cheaper, and more reliable digital logic modules — 3C instituted a company-funded, analytical study to evaluate all implications of this relatively new technology and determine its present and future effect on the general electronics industry. Broad

INDUSTRY REPORT CONTINUED ON PAGE 2

3C PULSE

VOLUME III, NUMBER 1

3C Pulse is a controlled circulation quarterly publication of Computer Control Company, Inc., Old Connecticut Path, Framingham, Massachusetts.

INTEGRATED CIRCUIT MODULES INTRODUCED AT IEEE

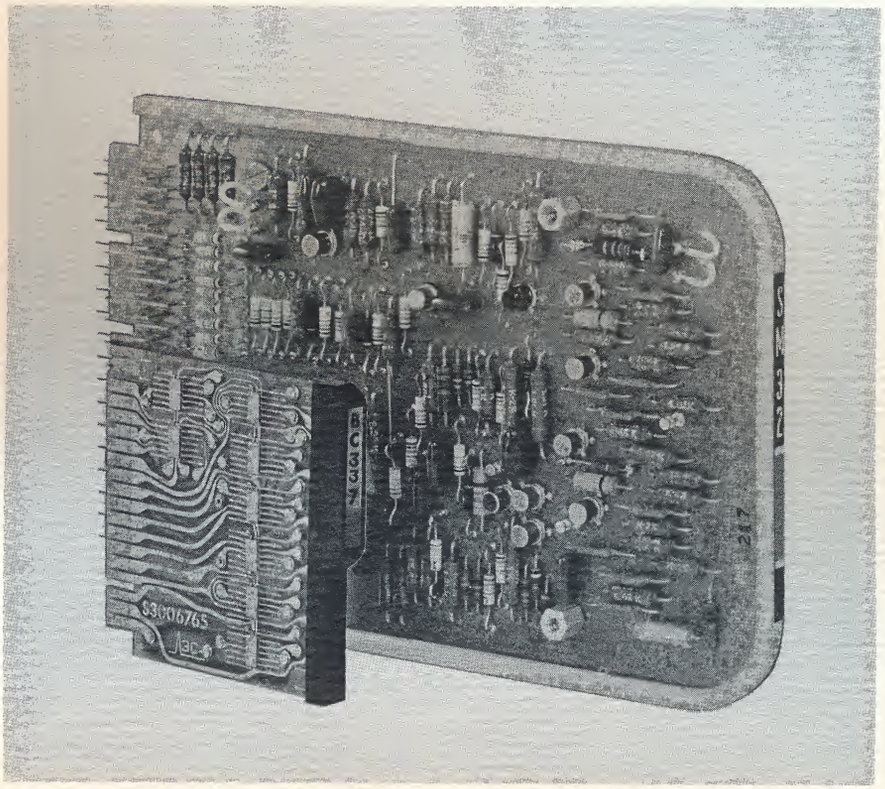
μ-PAC™ — A broad line of 5 mc monolithic integrated circuit modules was introduced at the IEEE International Convention in New York City, March 22-25. Supplementing the fully integrated line were hybrid (integrated/discrete) modules and a few purely discrete modules.

Twenty months of in-house funded research and design went into the 3C development of standard μ-PAC integrated logic packages which have flexibility of 3C's long-established discrete package lines. This was achieved while retaining price, size and reliability advantages inherent in integrated circuitry.

μ-PACS are integrated circuits mounted on etched glass-impregnated epoxy cards. With all circuit inputs and outputs available at connector pins, they make possible traditional systems design and permit design modification and simplified procedures for check-out and maintenance. Design changes or system expansion can be achieved by changing or adding modules and wiring. Any 3C module can be replaced from a small inventory of spares.

The etched printed circuits have gold-plated fingers for mating to 34-pin polarized connectors. PAC type is clearly indicated on a molded nylon handle by model number and color code.

Auxiliary equipment includes BLOCS for accepting wire wrap or taper pin connectors, power supplies, cooling units module extractors, extender PACS, manuals and logic sticker kits.



μ-PACS are integrated monolithic 5 mc circuit modules. They combine low price, size, and reliability advantages of microcircuits with the traditionally straightforward logic implementation, simplicity of design, and ease of use of the 3C S-PAC line.

μ-Pac Logic

μ-PAC circuits, operating from DC to 5 mc, utilize the NAND function, a method initially employed in 3C S-PACS, for positive logic. μ-PACS can also be used to directly implement the NOR function for negative logic, or AND-OR logic.

3C chose the universally accepted NAND operator for positive logic for its μ-PAC family of digital modules because of simplicity and usage symmetry made possible by the basic NAND gate circuit.

All modules are directly compatible, with no intermodule coupling. Trailing edge triggering of flip-flops via clock inputs provides intrinsic pulse dodging. There is no need for intervening networks or components.

Reliability

3C has drawn on 10 years' reliability experience with digital modules to design and develop a sound product line. To achieve optimum reliability, extensive consideration was given to circuit design approaches, component values, component tolerances, margins, heat transfer and performance specifications.

Inherent advantages contributing to the reliability of integrated circuits are:

- The industry proven planar epitaxial process.
- The greatly reduced number of thermal compression bonds required on a typical digital integrated circuit.
- The reduced number of component interconnections.
- The reduced number of sealed packages per circuit.
- Less variability between individual integrated circuits.
- Simpler production assembly of modules.
- Fewer testing programs required, hence easier traceability of defective circuits.

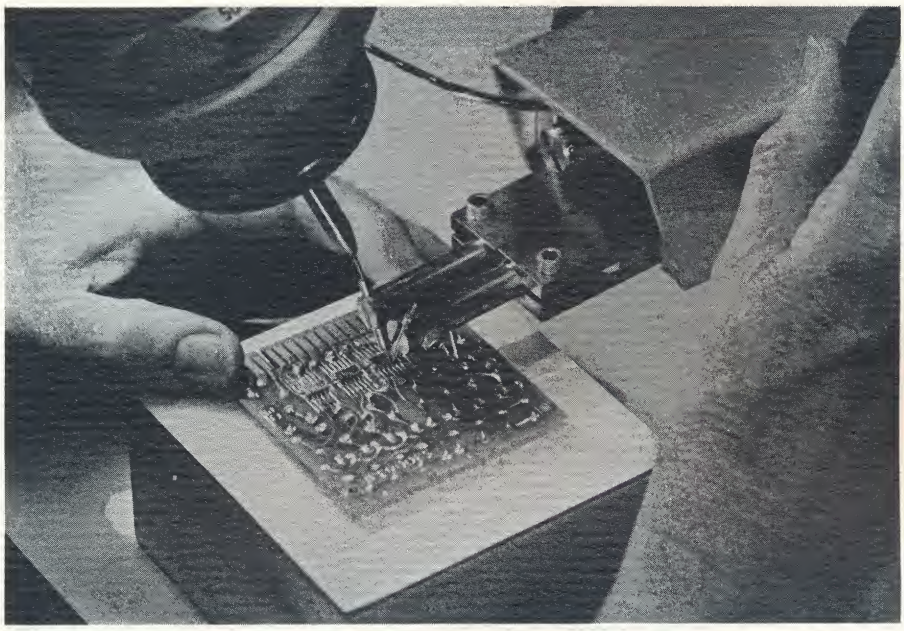
Hybrid circuits employ high quality, high stability discrete components, as used in other 3C module products. All semi-conductor components are silicon.

The wire wrap connector contains a precious metal tip contact welded to a phosphor bronze terminal. Contacts mate with the module's gold-plated printed circuit terminals. The taper pin connector has a gold-plated leaf type contact.

Rigid inspection, testing and overall quality assurance programs are an integral part of the μ-PAC manufacturing process.

Currently on life test at 3C are integrated circuit chips used in the μ-PAC line. The circuits employed are NAND gates and NAND gates

(continued on page 4)



Integrated circuit flat packs are attached to glass epoxy module cards by reflow soldering process. Resistance soldering machines guarantee reliable connections of flat packs to card by controlling rate and degree of heat, amount of pressure and rate of cooling.

(Continued from inside front cover)

areas of investigation included circuit design, logic design evaluation, packaging, fabrication techniques, and other appropriate areas of study.

In further support of these studies, 3C established a fully equipped and staffed microelectronic techniques laboratory. During the course of study, 3C laboratory scientists investigated all forms of microelectronic circuitry to evaluate every possible technique and their respective required trade-offs.

The laboratory staff evaluated thick films, thin films, monolithic integrated circuits, and hybrid circuits (the combination of one or more of the previous techniques or the combination of one or more of those techniques with various types of discrete components).

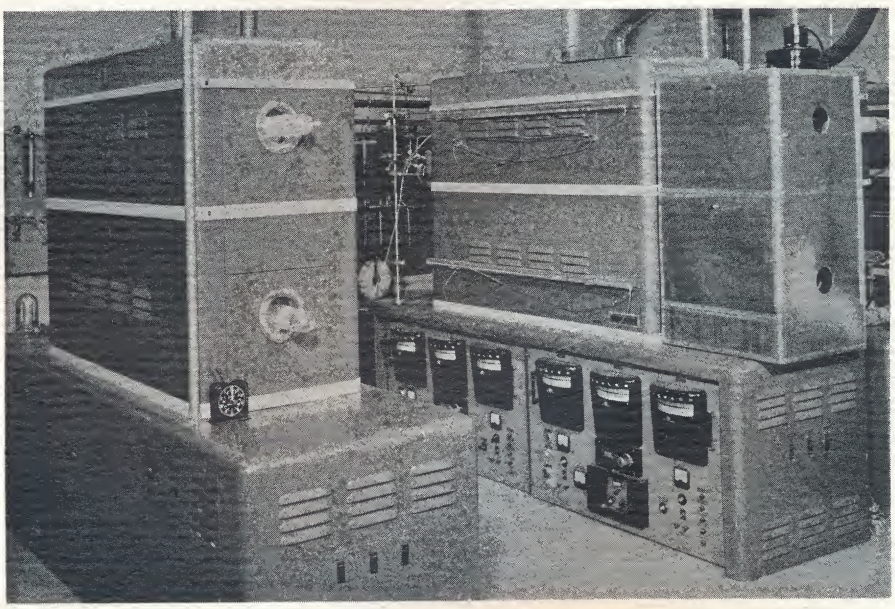
Simultaneously, 3C circuit design engineers analyzed and evaluated specific integrated circuits commercially available to industry. They tested characteristics, flexibility, and usability of each of these integrated circuits. 3C circuit design engineers also investigated various trade-off options in the design of digital circuits. They developed a capability for responding to various limitations in types of components, values, and tolerances. As the program matured, design breadboards of discrete components for various prototypes were built in conformance with the trade-offs determined by the techniques laboratory group.

Mechanical engineers drew upon extensive past product experience in the recommendation of appropriate size, shape, and configuration of related integrated circuit module equipment. They investigated the overall question of packaging to determine whether to combine our cordwood capability with microelectronics, or go for still greater packaging economies. Interconnection schemes (including backboard wiring build-up in various logic configurations) and the capabilities of wire wrap, solder, push-on and taper pin type connections were investigated. In addition, various types of materials for boards and cordwoods were examined, as well as multi-layer and double-sided printed circuit techniques, and the interconnection and mounting methods for the microcircuits.

3C computer and systems engineers determined logical capabilities of microcircuits used in different digital systems. They also examined historical logic configurations in order to assist in specifying necessary parameters for the proposed 3C product line.

By mid-1964, the techniques laboratory group had largely completed their evaluation of various microelectronic alternatives. They had developed the equipment and capability for producing not only components, but complete digital circuits. By achieving this capability, they were able to present to the circuit design group detailed restrictions and trade-off parameters for each type of microelectronic circuit. Similarly, circuit designers were capable of determining the 3C capability for design of specific general purpose product circuits within the trade-off specifications outlined by the techniques laboratory.

Today, μ-PAC is in production.



Fully equipped microelectronic techniques laboratory includes precisely controlled, high temperature diffusion furnaces used in the development of integrated circuits. Raw silicon wafers placed in these furnaces are subjected to gaseous atmospheres under extremely high temperatures to form circuit elements.

LABORATORY FACILITIES

Major 3C laboratory facilities include mask making, slide processing, photolithographic processing, thin film, and test equipment.

The mask making facility is capable of maintaining ±30 micron accuracy in original drafting on coated glass or mylar. Equipment is available for reduction and repetition of patterns in XY coordinates to an accuracy of ±1 micron. Photographic processing is performed in a temperature controlled sink. Line width of completed patterns can be held to ±0.8 micron.

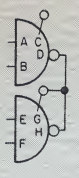
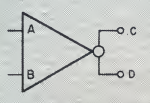
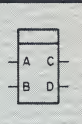
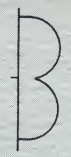
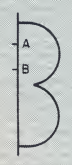
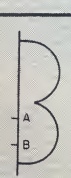
The slide processing area performs diffusion, epitaxial and photolithographic processes necessary for the fabrication of integrated circuits and other silicon semiconductor devices. Diffusion ovens perform oxidation and diffusion of phosphorous, boron, arsenic and gold. The epitaxial capability is equipped for depositing N and P type layers, hydrogen chloride vapor etching or oxide deposition by the carbon dioxide process.

Photolithographic processing is performed in a clean box with tolerances held to ±1 micron either on silicon or thin film glass substrates. Metalization is performed in a standard oil pumped vacuum system. For assembly and test of completed slices, a complete range of precisely controlled equipment is available including interferometers, microscopes, and probe equipment.

Thin film work is performed in an ion-pumped vacuum system with an electron gun for evaporation of materials. It has the capability of depositing films of alloys and refractory materials without significant distillation effects. A laser microscope can be used for tailoring thin film resistors.

Test equipment is available for measuring the characteristics of active and passive devices at frequencies up to 2000 mc. Specialized equipment is also available for measuring the pulse characteristics of active devices and some of the parameters in completed integrated circuits.

μ-PAC SYMBOLOGY

Symbol	Explanation	Boolean Expression (For Positive Logic)
	NAND Gate	$C = \overline{AB}$
	Diode cluster for expanding PAC inputs, node output n is actually only one connector pin.	$n = AB$
	NAND gate with node input n is for expansion of inputs with diode cluster. Node input shown twice to simplify expansion.	$C = \overline{ABn}$
	NAND gate with separate load circuit for paralleling gate outputs without decreasing drive capability. The paralleled gate outputs perform an AND operation for ONES and OR operation for ZEROS.	$D = H = \overline{AB+EF} = \overline{AB} \cdot \overline{EF}$
	Power Amplifier	$C = D = \overline{AB}$
	Basic flip-flop	$C = \overline{A}+ABC'$ $D = \overline{B}+ABD'$ where ' indicates previous state, and for $\overline{AB} = 1$, $C' = \overline{D}'$
J-K Flip-Flop Input Descriptions		
Symbol	Type Input	Explanation
	DC set or reset inputs	OR gate for ZEROS ($\overline{A}+\overline{B}$) or NAND gate for ONES ($\overline{AB}$)
	Clock input	
	Set control inputs	AND gate for ONES (AB)
	Reset control inputs	AND gate for ONES (AB)

(continued from page 1)

wired as flip-flops. The system consists of 60 circuits, wired in a continuous running, self-checking series system. A continuous train of clock pulses is sent through the string of circuits whose frequency is divided by two at each flip-flop. A lamp gives visible indication of system operation.

As of March 15, 1965, this system has operated 4,098 hours, or 245,880 circuit hours, without failure. (Life test program details are available on request.)

Mechanical

μ–PAC modules are monolithic integrated circuit assemblies supplemented by some discrete hybrid combinations mounted on 2.9 x 2.7 x .24 inch glass-impregnated epoxy cards. Each PAC type is clearly indicated by both model number and color code on the molded nylon handle. All PACS feature gold-plated etched fingers to guarantee reliable electrical contact with a 34-pin polarized connector.

Individual integrated circuits are assembled in 14-lead, .250 x .125 x .065 inch flat packs soldered to the etched wiring. Up to 22 flat packs can be mounted on a single μ-PAC card for counting or shift register operations. Resistance soldering methods enable simple replacement of components.

μ-PAC modules plug into precious metal wire wrap or taper pin connectors assembled in standard μ-BLOCS which permit flexible, low-cost backwiring techniques. Wire wrap terminals can employ other contact methods such as push-on, stackable contact, soldering, and percussion welding.

Power and ground pins are factory prewired in all μ-BLOCS with laminated copper and epoxy glass distribution lines. A low impedance clock distribution line is also provided. The copper and glass planar arrangement permits maximum decoupling of spurious signals from power and ground lines. Connector plane and power bus assembly can be easily removed from the μ-BLOC to permit convenient bench wiring of system logic.

Built-in cooling units are contained in each BLOC. The BLOC cooling system is designed so that temperature rise within an integrated circuit will be well within specified limits when outside ambient temperature of the BLOC is within the rated 55°C. When two BLOCS are used together in a cabinet, it is possible to arrange the units to make fans work in a push-pull manner.

Plug-in power supplies are designed for easy BLOC insertion and removal. The line also includes rack mountable power supply for driving a series of BLOCS.

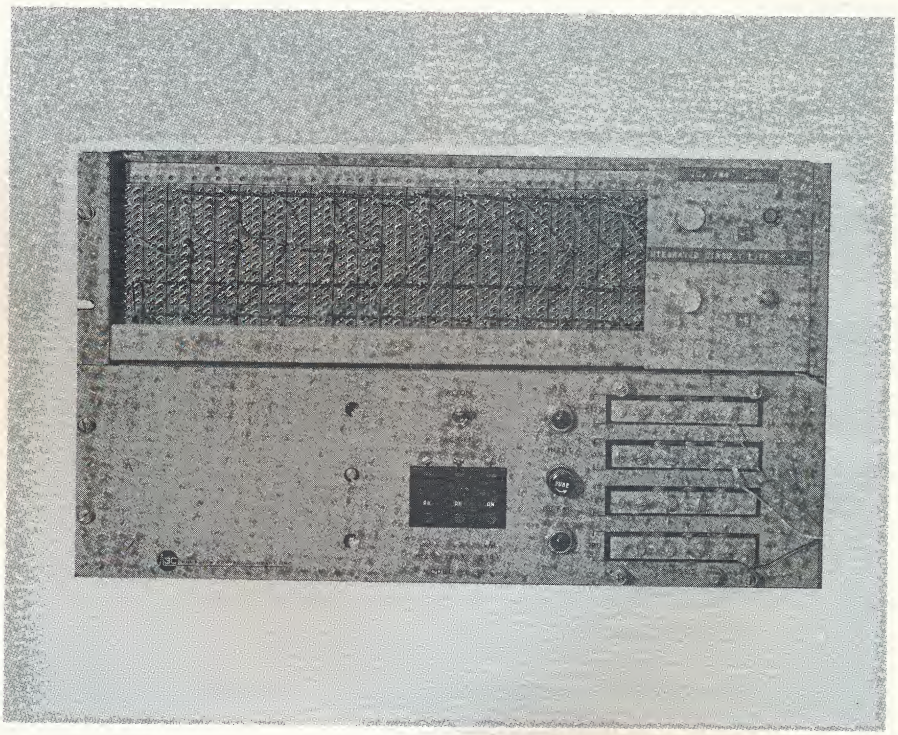
Electrical Characteristics

μ-PAC is a static asynchronous digital logic line similar to S-PAC. Diode transistor logic (DTL) is employed for its noise rejection, speed and expandable input capabilities. Circuit designs meet the specification needs of a 5 megacycle product line featuring input gate expansion, output cascoding, high fan-out, high noise thresholds, and low propagation delays.

The basic logic unit, the NAND gate, performs a NAND function for positive logic and a NOR function for negative logic. Inputs are generally expandable by addition of diode clusters available on selected gate modules.

Most flip-flop μ-PACS utilize a single, versatile, flip-flop circuit. This basic circuit is a double rank J-K flip-flop. The double rank approach uses two flip-flops to perform AC operations. The AC gate portion of the flip-flop is composed of the clock input and the set and reset control inputs. Control inputs are activated by logical ONES (not logical ZEROS as in S-PACS). A ZERO-ONE-ZERO pulse on the clock will cause the flip-flop to assume the state determined by the condition of the control inputs, there being no ambiguous state with J-K circuitry.

Information is entered into the first flip-flop on one transition of the clock input and is shifted to the second flip-flop on the other clock



Integrated circuits, designed and developed by 3C, undergo life test in a typical system application. This self-checking system has operated continuously for more than 250,000 circuit hours without a single component failure. Continuous life test programs are performed as part of 3C's extensive μ-PAC reliability program.

transition. The clock inputs provide intrinsic pulse dodging by means of trailing edge triggering. This feature permits strobing of the flip-flop output with input signals. DC set and reset inputs are also available and override any activity in the AC portion of the flip-flop. Versatility is evident in the set and reset control inputs which may be utilized (1) as direct inputs, (2) to steer clock pulse, or (3) when tied together, as a clock input. A patent application is on file for this flip-flop circuit. In addition, a flip-flop consisting of two cross-coupled NAND circuits is used to provide an RS type flip-flop module.

The Power Amplifier PAC adds high drive capability gating to the line with the added feature of short delay time. Built-in short circuit protection (patent applied for) limits the output current when the output is short circuited.

Other electrical features:

1. All logic circuits operate from a single voltage source of +6 volts. Power supplies provide current at +6 volts and also supply current at —6 volts for auxiliary circuits such as the Multivibrator Clock, Master Clock or the Schmitt Trigger.
2. Input noise rejection is 1.35 volts typical.
3. All μ-PAC circuits are DC coupled.
4. Excessive stray capacitance loading will slow down circuit operation but will not cause failure.
5. Signal levels are nominally 0 volts for logical ZERO and +6 volts for logical ONE.
6. All inputs are diode coupled/isolated.
7. Loading numbers are expressed in easy-to-use unit numbers, and include wide safety margins at maximum operating frequency. In addition to indicated fan-out, ample margin is included for the specified stray capacitance to permit greater freedom in PAC-to-PAC wiring. Nominal μ-PAC unit load is 1.6 milliamperes.
8. Listed performance specifications are based on "worst case" stack-up of tolerances. Performance will usually exceed these specifications considerably.
9. All modules have standard power input connections.

GENERAL μ-PAC SPECIFICATIONS

Frequency	DC to 5 MC
Logic Levels:	
Logic ONE	+2.5 volts to +6.3 volts (or an open circuit at the input)
Logic ZERO	0 volt to 1.0 volt
Noise Rejection	1.35 volts, typical
Ambient Operating Temp. Range	0°C to +55°C
Storage Temperature Range	—65° to +150°C
Power Supply Voltage	+5.1 volts to +6.3 volts (—6 volts also necessary on some auxiliary non-logic circuits)

NAND GATE PAC SPECIFICATIONS

Input Loading	1 unit load
Fan In	12
Fan Out	8
Stray Capacitance	40 picofarads
Circuit Delay (measured at +1.5 volts, averaged over 2 stages):	23 nanoseconds, typical

J-K FLIP-FLOP SPECIFICATIONS

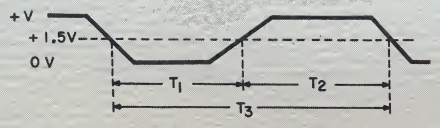
Inputs	
DC Set Input	⅔ unit load
DC Reset Input	⅔ unit load
Clock	1 unit load
Control	1 unit load
Fan Out	8
Stray Capacitance	40 picofarads
Circuit Delay (measured at +1.5 volts)	
Clock input to flip-flop output	60 nanoseconds, maximum
DC Set input to set output	80 nanoseconds, maximum
DC Set input to reset output	60 nanoseconds, maximum
Set control input to set output	60 nanoseconds, maximum
Set control input to reset output	60 nanoseconds, maximum

POWER AMPLIFIER SPECIFICATIONS

Input Loading	2 unit loads
Fan In	12
Output Drive Capability	25 loads plus 250 picofarads
Circuit Delay (measured at +1.5 volts, averaged over 2 stages)	23 nanoseconds, typical

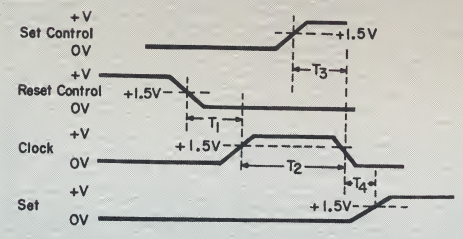
μ – PAC WAVEFORM CHARACTERISTICS

In reviewing waveforms, the following definitions will apply: Negative time — signal duration below +1.5 volts. Positive time — signal duration above +1.5 volts. Timing is measured and specifications set at the +1.5 volt circuit switching point. Since all μ-PAC circuitry is DC coupled, Rise and Fall Time specifications are less important. Set and reset inputs denote voltage levels and appear at the output of gates and flip-flops. Assertion and Negation outputs denote pulses and appear at the output of clocks and delay multivibrators.



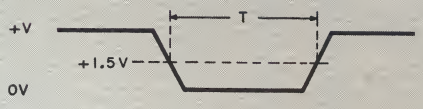
ACTIVATION OF CLOCK INPUT

Negative time (T_1) = 60 nanoseconds, minimum
Positive time (T_2) = 40 nanoseconds, minimum
Voltage (V) = +2.5 volts, minimum



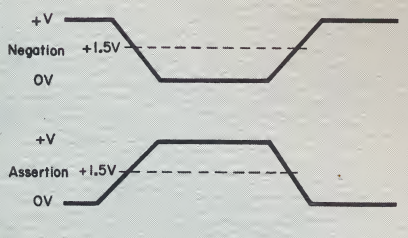
TIMING OF CONTROL INPUTS (When used to steer clock pulse*)

Negation time of control input before clock pulse goes positive (T_1) = 0 nanoseconds, minimum
Positive time of clock pulse (T_2) = 40 nanoseconds, minimum
Positive time of control input before clock pulse goes negative (T_3) = 40 nanoseconds, minimum
Time from negative clock transition to set output (T_4) = 60 nanoseconds, maximum
Voltage (V) = +2.5 volts, minimum
No control input should go from +V to 0 volts while clock is at +V.
*When control inputs are used as a clock input, refer to "activation of clock input" waveform.



ACTIVATION OF DC SET AND RESET INPUTS

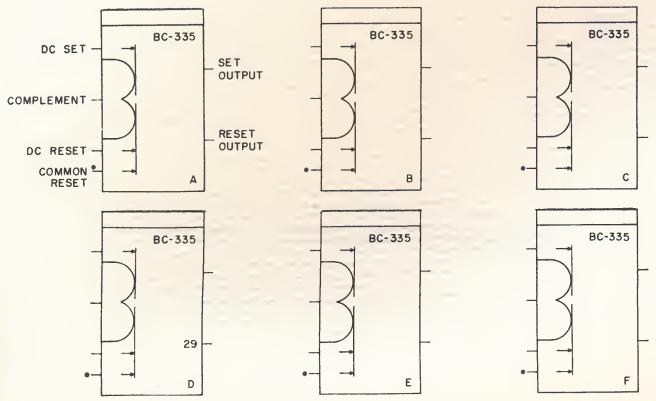
Negative time (T) (clock in ZERO state) = 80 nanoseconds, minimum
Negative time (T) (clock in ONE state) = 60 nanoseconds, minimum
Voltage (V) = +2.5 volts, minimum



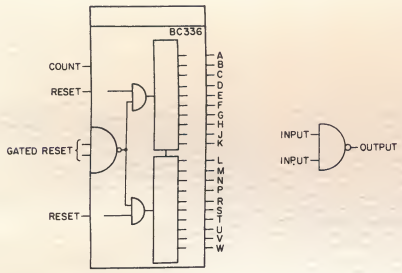
OUTPUT PULSE CHARACTERISTICS

Pulse duration (T) = 50 nanoseconds, nominal
Voltage (V) = +3.5 volts, minimum

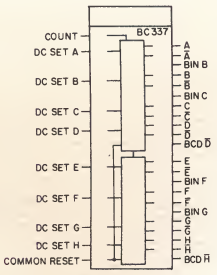
μ – PAC DESCRIPTIONS



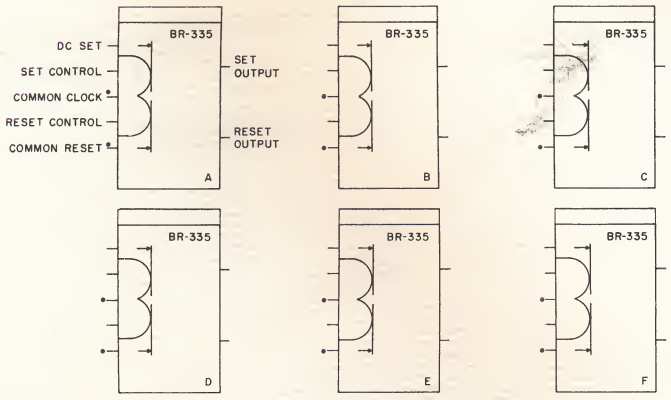
6 FLIP-FLOPS FOR BINARY COUNTING



8 TO 20 FLIP-FLOPS PREWIRED FOR BINARY COUNTING

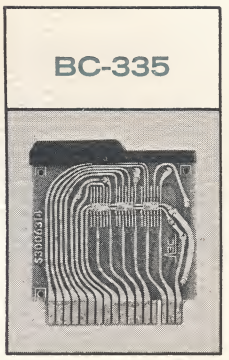


8 FLIP-FLOPS FOR BINARY OR BCD COUNTING



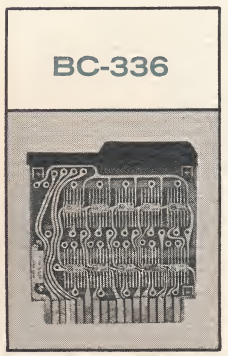
6 FLIP-FLOPS PREWIRED WITH COMMON CLOCK AND COMMON RESET INPUT

BC-335 COUNTER PAC



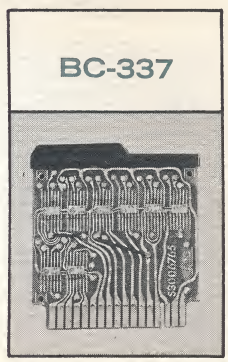
Counter PAC, BC-335, contains six independent flip-flops with appropriate inputs for operation as binary counters. They may also be employed individually as complementing flip-flops. The common reset line is shared by all circuits. Typical uses of the Counter PAC include up or down counting, frequency division and buffer storage.

BC-336 BINARY COUNTER PAC



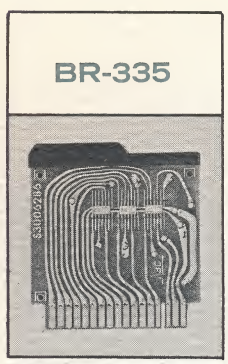
Binary Counter PAC, BC-336, contains between 8 and 20 prewired binary counter stages. The number of stages is determined by the user. This high density module can be used for counting and frequency division. By application of a single reset signal or gated reset signals to the common reset gating, all stages of the counter can be reset. The set output at each state is accessible at PAC terminals.

BC-337 FAST CARRY COUNTER PAC



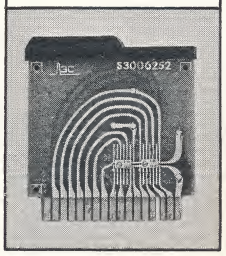
Fast Carry Counter PAC, BC-337, contains an eight stage prewired counter which can be easily converted to a binary counter or BCD counter by using jumper connections. A count input is available at the input of the first stage. Each stage has a DC set which allows for presetting any desired number in the counter. A common reset is available for clearing all stages simultaneously.

BR-335 BUFFER REGISTER PAC



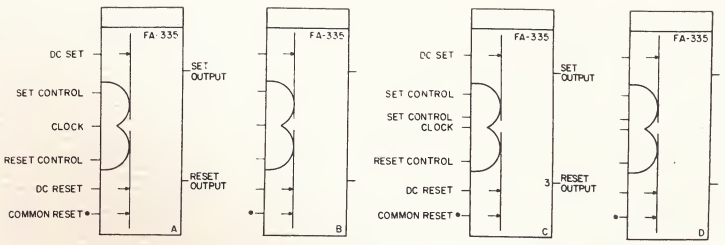
Buffer Register PAC, BR-335, contains six flip-flops with independent set-reset capability. Available set-reset inputs allow for parallel loading of information. Common clock and common reset inputs make possible simultaneous operations on all stages. Typical uses for the Buffer Register PAC include shifting, accumulating, and parallel transfer.

FA-335



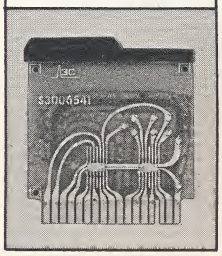
FA-335 GATED FLIP-FLOP PAC

Gated Flip-Flop PAC, FA-335, contains four independent flip-flops, each with AC and DC inputs and a common reset. The versatile input structure allows for control of the flip-flop from a variety of level and pulse inputs. Typical uses of the Gated Flip-Flop PAC include storage, counting, shifting, and parallel transfer.



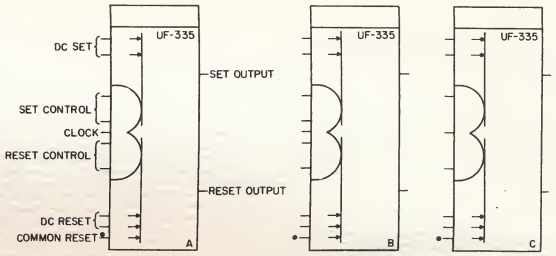
4 FLIP-FLOPS WITH DC, CLOCK AND CONTROL INPUTS

UF-335



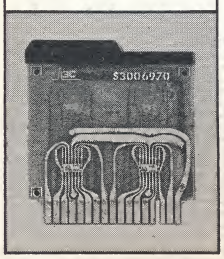
UF-335 UNIVERSAL FLIP-FLOP PAC

Universal Flip-Flop PAC, UF-335, contains three independent flip-flops each with AC and DC input gating and a common reset. With this complete range of inputs, these flip-flops can perform all the functions of other μ-PAC flip-flops plus many additional logic operations. Typical uses of the Universal Flip-Flop include storage, complementing, up/down counting, shifting, control, accumulating, and parallel transfer.



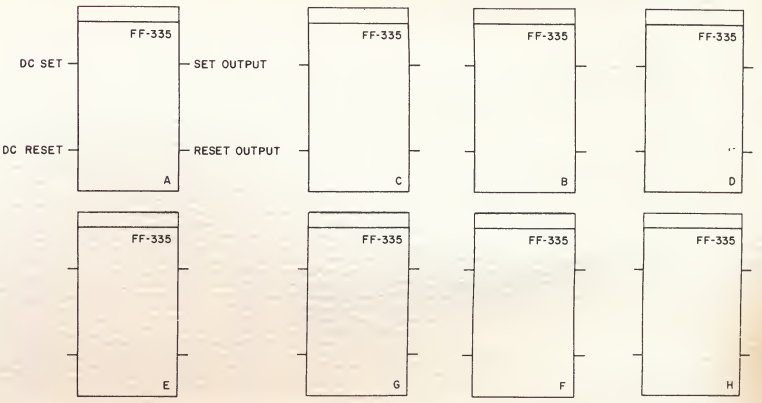
3 FLIP-FLOPS WITH AC AND DC INPUT GATING

FF-335



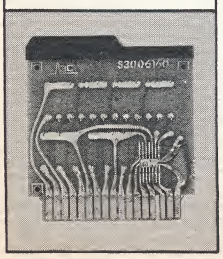
FF-335 BASIC FLIP-FLOP PAC

Basic Flip-Flop PAC, FF-335, contains eight independent flip-flops. Each stage has a DC set and reset input and a set and reset output. The circuit consists of two NAND gates internally wired back-to-back. The Basic flip-flop is used for economical implementation of logic operations which do not require additional flip-flop inputs, such as input-output registers, storage, and buffering applications.



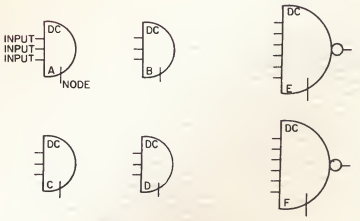
8 FLIP-FLOPS WITH DC INPUT GATING

DC-335



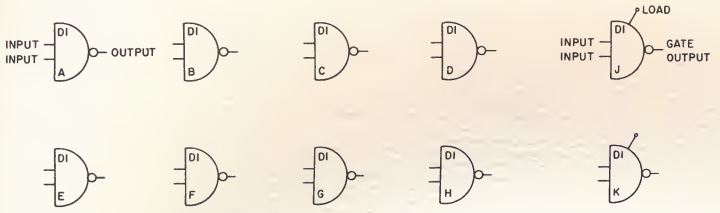
DC-335 MULTI-INPUT NAND PAC

Multi-Input NAND PAC, DC-335, contains 2 six-input NAND gates with nodes and 4 three-diode clusters. Gate node input allows for expansion of the number of gate inputs by attachment of diode clusters.



4 THREE-INPUT DIODE CLUSTERS

2 SIX-INPUT NAND GATES WITH NODES

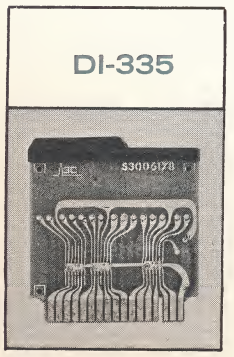


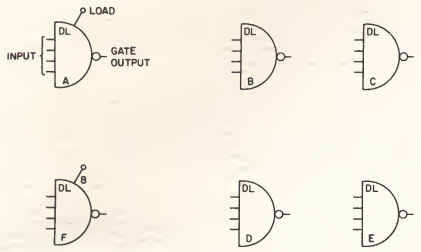
8 TWO-INPUT NAND GATES

2 TWO-INPUT NAND GATES WITH SEPARATE LOAD CIRCUITS

DI-335 NAND PAC

NAND PAC, DI-335, contains 10 two-input NAND gates. Two of the gates have collector loads separate from the collector outputs. By tying the gate outputs to a single load circuit, a number of gates can be connected in parallel without reducing output drive capability.



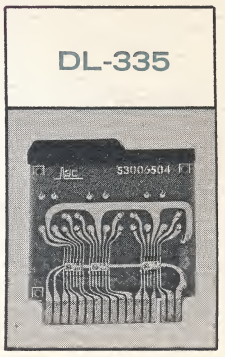


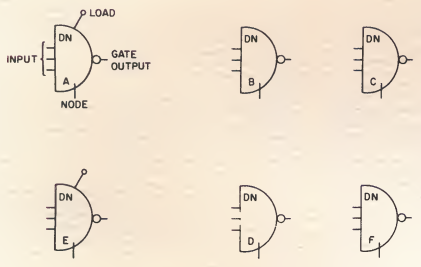
4 FOUR-INPUT NAND GATES

2 FOUR-INPUT NAND GATES WITH SEPARATE LOAD CIRCUITS

DL-335 NAND TYPE 2 PAC

NAND Type 2 PAC, DL-335, contains 6 four-input NAND gates. Two of the gates have disconnected collector load resistors which are brought out on separate terminals. By tying the gate outputs to a single load circuit a number of gates can be connected in parallel without reducing output drive capability.



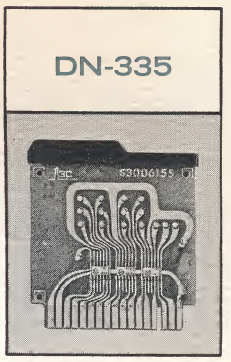


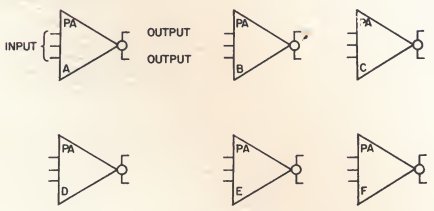
4 THREE-INPUT NAND GATES WITH NODES

2 THREE-INPUT NAND GATES WITH NODES AND SEPARATE LOAD CIRCUITS

DN-335 EXPANDABLE NAND PAC

Expandable NAND PAC, DN-335, contains 6 three-input NAND gates with nodes. Two of the gates have disconnected load resistors which are brought out on separate terminals. By tying gate outputs to a single load circuit, a number of gates can be connected in parallel without reducing output drive capability. Gate node input allows for expansion of the number of gate inputs by attachment of diode clusters.

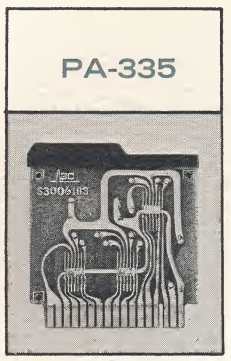




6 THREE-INPUT INVERTING POWER AMPLIFIERS

PA-335 POWER AMPLIFIER PAC

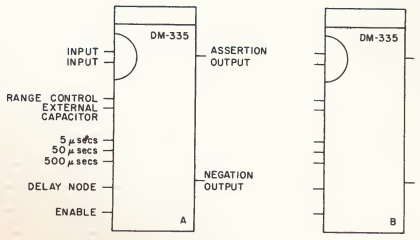
The Power Amplifier PAC, PA-335, contains 6 three-input high-drive NAND gates, each capable of driving 25 unit loads and 250 picofarads stray capacitance. Each gate has two electrically common outputs to reduce load distribution current on any single wire. Built-in short circuit protection limits output current when the output is accidentally grounded.



DM-335

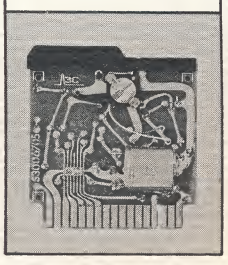
DM-335 DELAY MULTIVIBRATOR PAC

The Delay Multivibrator PAC, DM-335, contains two independent monostable (one shot) multivibrators capable of generating assertion and negation pulses in a variety of widths. Each circuit has two NAND inputs, an Enable and three discrete variable delay taps to vary output pulse width from 100 nanoseconds to 500 microseconds. External capacitors can be used to obtain pulse widths up to several seconds.



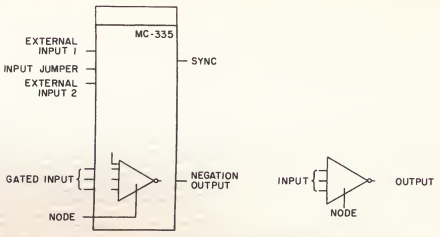
2 MONOSTABLE MULTIVIBRATORS, STEP ADJUSTABLE PULSE WIDTH

MC-335



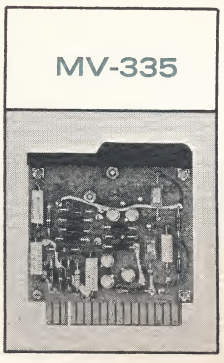
MC-335 MASTER CLOCK PAC

Master Clock PAC, MC-335, contains a crystal controlled oscillator, a pulse shaper and a pulse amplifier. The oscillator operates between 200 kc and 5 mc and can be driven by an external frequency source when the crystal is removed. The pulse shaper section can vary pulse width between 50 to 150 nanoseconds by means of a built in potentiometer-capacitor network. Pulse width can be increased further by use of external capacitors.



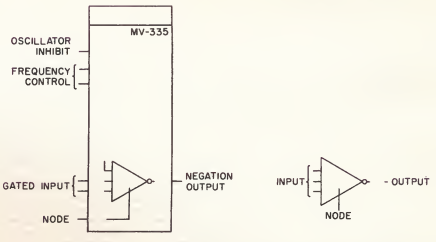
1 CRYSTAL-CONTROLLED CLOCK

MV-335



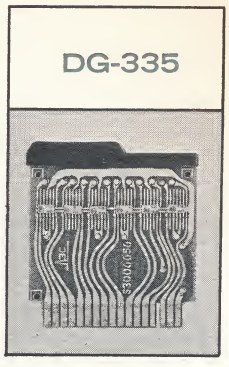
MV-335 MULTIVIBRATOR CLOCK PAC

Multivibrator Clock PAC, MV-335, contains a free-running variable frequency multivibrator, a pulse shaper and a pulse amplifier. The free-running multivibrator operates between 200 kc and 5 mc. Frequency and pulse widths can be varied by means of potentiometer-capacitor networks. Oscillator inhibit is used to provide synchronous start/stop capability from external asynchronous signals.



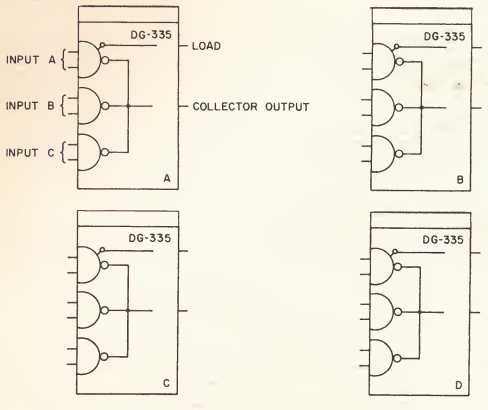
1 FREE-RUNNING MULTIVIBRATOR CLOCK

DG-335

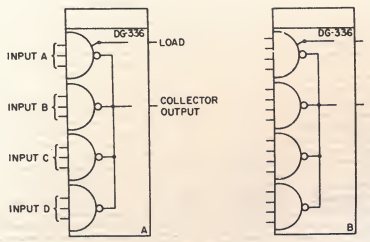


DG-335 SELECTION GATE TYPE 1 PAC

Selection Gate Type 1 PAC, DG-335, contains four independent functional gate structures. Each gate structure has 3 two-input NAND gates and performs the AND-OR-INVERT function. It can be used for transfer control of three data signals. By tying the various gate structures to a common load, gating arrangements for the transfer control of up to twelve signals can be performed. Only one transfer line is activated during the transfer time period.



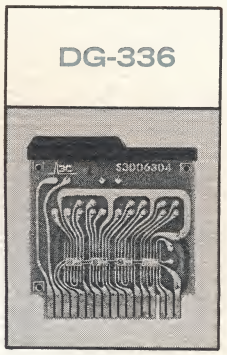
4 SELECTION GATE STRUCTURES

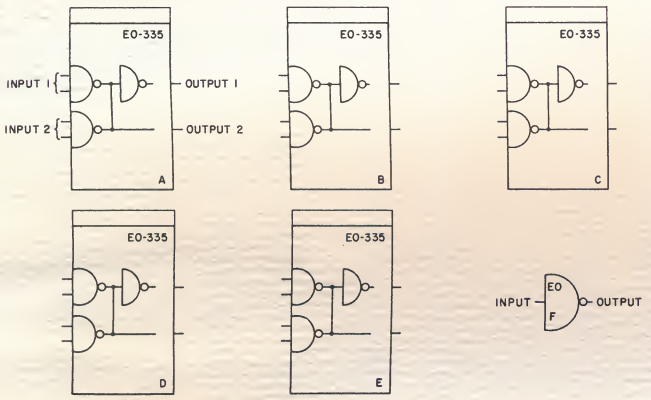


2 SELECTION GATE STRUCTURES

DG-336 SELECTION GATE TYPE 2 PAC

Selection Gate Type 2 PAC, DG-336, contains two independent functional gate structures. Each gate structure has 4 three-input NAND gates and performs the AND-OR-INVERT function. It can be used for transfer control of four sets of data signals. By tying the various gate structures to a common load, gating arrangements for the transfer control of up to eight sets of data signals can be performed. Only one transfer line is activated at a time.

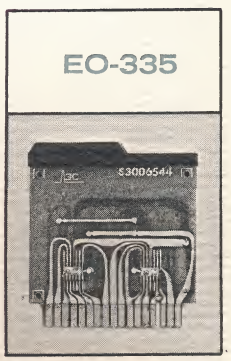


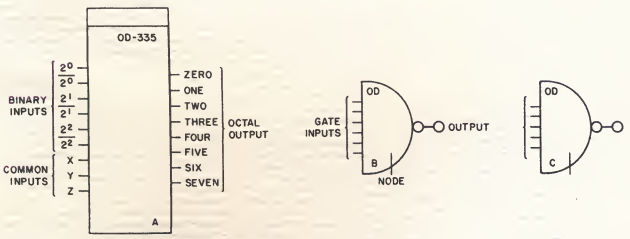


5 EXCLUSIVE OR GATE STRUCTURES WITH 1 ONE-INPUT NAND GATE

EO-335 EXCLUSIVE OR PAC

Exclusive OR PAC, EO-335, contains five independent functional gate structures and one independent NAND gate. Each gate structure contains 3 two-input NAND gates and performs AND-OR and AND-OR-INVERT functions. Gate structures can be used for sensing the exclusive OR and for sensing equality of two inputs.

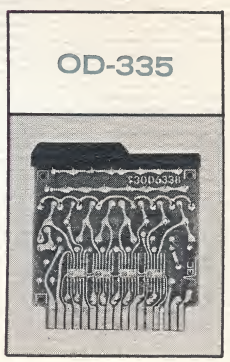


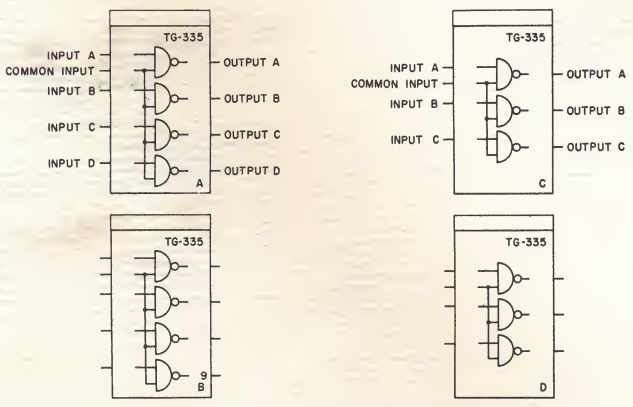


1 PRE-WIRED BINARY-TO-OCTAL DECODER

OD-335 OCTAL/DECIMAL DECODER PAC

Octal/Decimal Decoder PAC, OD-335 contains a prewired binary-to-octal decoder and two additional independent NAND gates to expand the matrix for BCD-to-decimal decoding. Three additional input lines are available for expanding the matrix from 8 to 16, 32, or 64 outputs by use of additional OD-335 PACS.

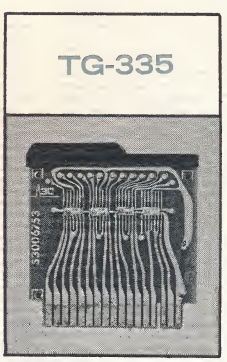


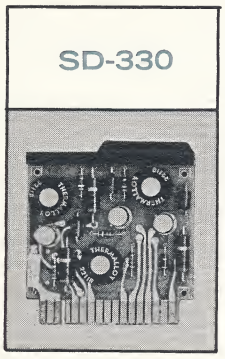


4 TRANSFER GATE STRUCTURES

TG-335 TRANSFER GATE PAC

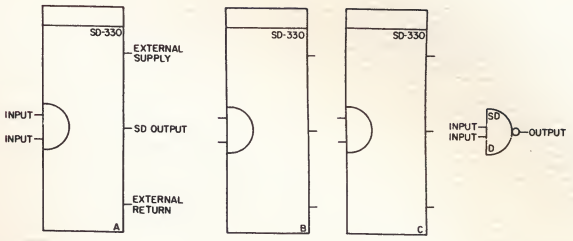
Transfer Gate PAC, TG-335, contains four independent functional gate structures. Two of the structures have 4 two-input NAND gates, one input on each gate being common to the four gates. The remaining two structures have 3 two-input NAND gates, one input being common to the three gates. Each gate structure can be used for the common transfer control of three or four data signals respectively.



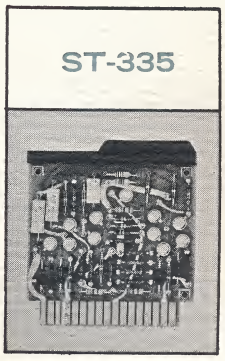


SD-330 SOLENOID DRIVER PAC

Solenoid Driver PAC, SD-330, contains three independent circuits for driving heavy resistive, capacitive or inductive loads. Each circuit has two NAND inputs and is capable of switching up to one ampere of current at 500 cycles per second from a positive supply of up to 28 volts. One independent two-input NAND gate is also included.

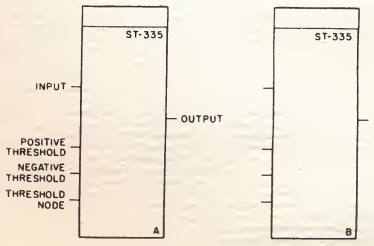


3 SOLENOID DRIVER CIRCUITS WITH ADDITIONAL GATE

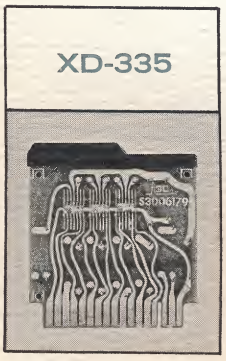


ST-335 SCHMITT TRIGGER PAC

Schmitt Trigger PAC, ST-335, contains two independent trigger circuits capable of converting various shaped inputs and one output. Switching levels can be varied from +2.5 volts to −2.5 volts by making appropriate pin connections. In addition, the circuit can perform signal attenuation, differentiation and integration by use of available resistor-capacitor stud mounts.

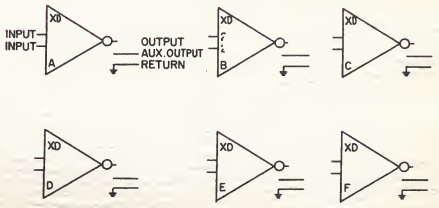


2 SCHMITT TRIGGER CIRCUITS

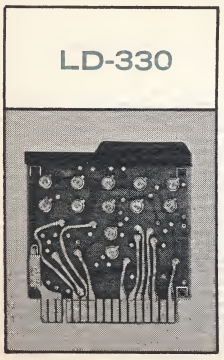


XD-335 TRANSMISSION LINE DRIVER PAC

Transmission Line Driver PAC, XD-335, contains 6 two-input driver circuits. Each circuit is capable of driving standard 50 ohm, 75 ohm and 93 ohm coaxial cables at repetition rates up to 5 megacycles. When transmission line termination other than the provided 62 ohms is required, the proper resistor can be mounted on available studs.

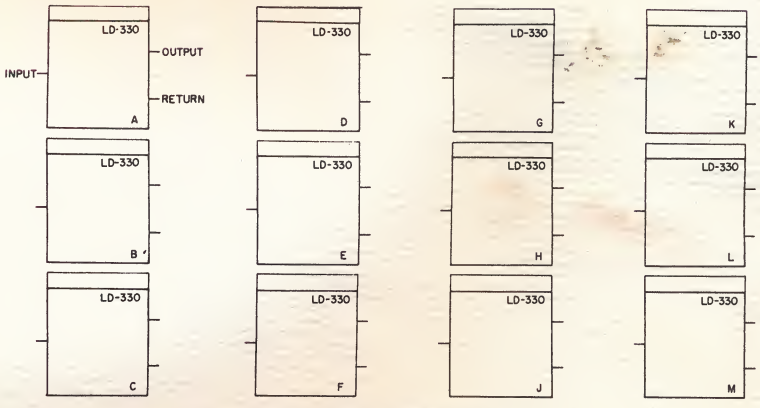


6 TWO-INPUT TRANSMISSION LINE DRIVERS



LD-330 LAMP DRIVER PAC

Lamp Driver PAC, LD-330, contains twelve identical independent lamp driver circuits. Each circuit is capable of switching 20 milliamps of current at any positive voltage up to 20 volts, at a maximum frequency of 1 mc.



12 INDICATOR LAMP DRIVER CIRCUITS

μ-BLOCS

Seven μ-BLOC models are available. All seven models use the same basic structure, but differ in width dimension, type and number of connectors. These BLOCS can be supplied with or without provisions for plug-in power supply unit. Mounting ears are detachable and allow for front or back mounting of the connector plane.

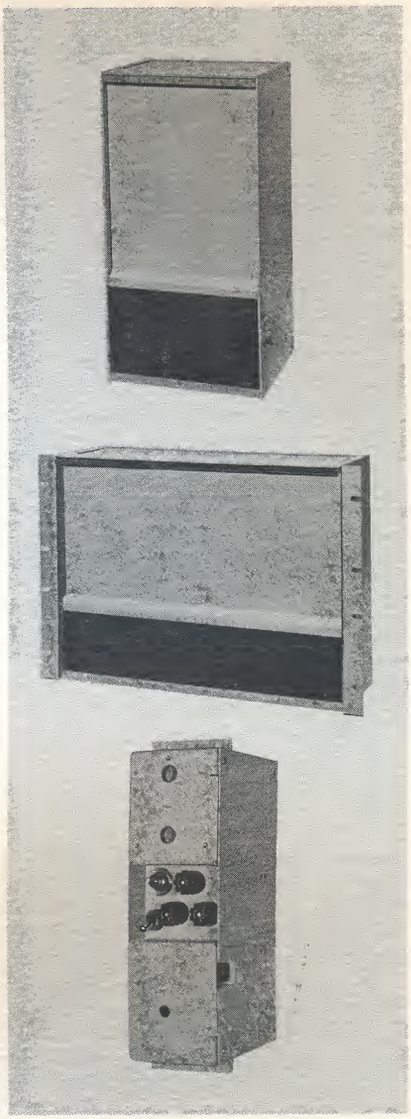
The BL series is directly mountable in standard 19 inch rack panel. BM-335 and BM-337 BLOCS can be adapted to mount in a 19 inch rack by using a mounting panel. If desired, this panel can then be used as a control panel. The BM-335 and BM-337 BLOCS can also be coupled for side-by-side mounting in a 19 inch rack.

Wire wrap or taper pin connectors are mounted in BLOCS with ground and power prewired. The connector plane is easily removable for convenient wiring.

Built-in cooling units are contained in each BLOC. When two BL series BLOCS are used together, the fans can be utilized in a push-pull manner.

Model	Number of Connectors	Dimension		
		W	H	D
BM-330	24 WIRE WRAP	6	12¼	5¼
BM-335	24 TAPER PIN	8½	12¼	5¼
BM-337*	36 TAPER PIN	8½	12¼	5¼
BL-330	96 WIRE WRAP	17	12¼	5¼
BL-331	48 TAPER PIN	17	12¼	5¼
BL-332*	144 WIRE WRAP	17	12¼	5¼
BL-333*	72 TAPER PIN	17	12¼	5¼

*Do not have provisions for a plug-in power supply unit



Plug-in Power Supplies

Plug-in Power Supplies, PB-330 and PB-331, are integrally packaged units that can be mounted directly into BLOCS. PB-330 mounts in BM BLOCS, PB-331 mounts into BL BLOCS. They supply current at both μ-PAC voltage levels, +6 and −6 volts, and are designed to drive all modules contained in their respective BLOCS. By making the necessary internal connections, these supplies can accommodate input voltages of 115 or 220 volts AC at standard input frequencies of 50, 60 and 400 cycles per second.

Front panels include the following features: on/off switch, power on indicator, three fuses, and voltage adjustment potentiometers.

Accessory μ-PAC equipment also available includes the XP-330 Extender PAC, JT-330 Jumper Lead Set (Taper Pin), Module Extractor, Automatic wire wrap kit, and both wire wrap and taper pin wiring tools.

SEE BACK COVER FOR 3C PAC LITERATURE AVAILABLE ON REQUEST

3C PAC LITERATURE AVAILABLE ON REQUEST

CATALOG μ-PAC-1 . . .

. . . documents new 5 mc μ-PAC™ integrated circuit modules. Catalog includes individual PAC descriptions, logic diagrams, and specifications. Also detailed: mounting hardware, power supplies module accessories, and designer aids.

CATALOG S-3 . . .

. . . details the full family of 3C S-PAC digital logic modules in frequency ranges of DC-200 kc, DC-1 mc and DC-5 mc. Catalog describes mounting hardware, power supplies, module accessories and designer aids.

CATALOG SIL-1 . . .

. . . describes SILICON S-PAC, 1 mc digital logic modules. Catalog describes mounting hardware, power supplies, module accessories, and designer aids.

CATALOG H-2 . . .

. . . details 3C H-PACS — a line of high speed logic modules which operate from DC-20 mc. Line includes wide selection of mounting hardware, power supplies, module accessories, and designer aids.

Please send more information on:

☐ New μ-PACS ☐ S-PACS ☐ Silicon S-PACS ☐ H-PACS

NAME .....

TITLE .....

FIRM .....

ADDRESS .....

CITY ..... **STATE** ..... **ZIP** .....

An indication of your particular requirements would be helpful.

My interest is:

- ☐ Have used discrete digital modules
- ☐ Am contemplating use of integrated circuit modules
- ☐ Have module requirement now
- ☐ Have future module requirement
  - 6 months ☐ 12 months ☐
  - 18 months ☐

My requirements involve:

- ☐ Specifically integrated circuitry
- ☐ High reliability
- ☐ Frequencies to ..... megacycles
- ☐ High environments
- ☐ High packaging density
- ☐ Ease of system modification/repair
- ☐ Other .....